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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00877 JW **DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF FOR THE "TOP TEN" TERMS** Date: January 27, 2012 Judge: Hon. James Ware

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00882 JW
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-05398 JW

Table of Contents

Table of Authorities

Cases

Table of Abbreviations

'148 patent	U.S. Patent No. 6,598,148, entitled "High Performance Microprocessor Having Variable Speed System Clock," issued July 22, 2003 (attached to the Otteson Decl. as Exhibit CC)
'336 patent	U.S. Patent No. 5,809,336, entitled "High Performance Microprocessor Having Variable Speed System Clock," issued September 15, 1998 (attached to the Otteson Decl. as Exhibit DD)
'749 patent	U.S. Patent No. 5,440,749, entitled "High Performance, Low Cost Microprocessor Architecture," issued August 8, 1995 (attached to the Otteson Decl. as Exhibit BB)
'890 patent	U.S. Patent No. 5,530,890, entitled "High Performance, Low Cost Microprocessor," issued June 25, 1996 (attached to the Otteson Decl. as Exhibit AA)
Alliacense	Declaratory judgment defendant Alliacense Limited
Asserted Patents	The '148, '336, '749 and '890 patents
Defendants or TPL	Declaratory judgment defendants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited (also collectively "TPL")
JCCS	Joint Claims Construction Statement, filed November 23, 2011 (*Acer* Dkt. 307); Exhibits to the JCCS were filed as *Acer* Dkt. 305
Mar Decl.	Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief, filed December 9, 2010 (*Acer* Dkt. No. 213)
Otteson Decl.	Declaration of James C. Otteson in Support of Defendants' Opening Claim Construction Brief for the "Top Ten" Terms
Patriot	Defendant Patriot Scientific Corporation
Plaintiffs	Declaratory judgment plaintiffs Acer, Inc., Acer America Corporation, Barco, N.V., Gateway, Inc., HTC Corporation and HTC America, Inc.
TPL	Defendant Technology Properties Limited; "TPL" is also used throughout this brief to refer to all three declaratory judgment defendants
Wolfe Depo.	Excerpts from the deposition of Andrew Wolfe, Ph.D., taken on November 12, 2010 (attached as Exhibit V to the Mar Declaration)

Introduction

Declaratory judgment defendants TPL, Patriot and Alliacense (collectively "TPL") respectfully ask the Court to enter their proposed constructions of the "Top Ten" claim terms in dispute. As discussed below, TPL's constructions most closely adhere to the intrinsic evidence and are supported by the applicable legal authorities that govern claim construction. By contrast, declaratory judgment Plaintiffs' competing constructions improperly incorporate limitations from the specifications of the Asserted Patents. Plaintiffs also improperly seek to further interpret the correct constructions that Judge Ward previously applied to some of the terms at issue.[1]

Factual Background

A. The Inventors – Charles Moore and Russell Fish – Revolutionized Microprocessor Technology With The Inventions Disclosed in the Asserted Patents.

Charles Moore and Russell Fish are the co-inventors of the pioneering patents at issue in this case: the '890, '749, '148 and '336 patents (Otteson Decl., Exhs. AA through DD, respectively). In 1988 and 1989, Moore and Fish designed a 32-bit microprocessor called "ShBoom," which the IEEE identified as one of "The 25 Microchips that Shook the World."[2] On August 3, 1989, the inventors filed a comprehensive patent application, from which seven patents, including the Asserted Patents, ultimately issued. Moore was inducted into the Computer Design Hall of Fame and received a Presidential commendation among other awards for his pioneering work in the computer industry. Over 90 global electronics firms (including Intel, Sony, HP and others) have now licensed the Moore patents from TPL, and the four Asserted Patents have withstood over ***sixteen*** reexaminations.

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[1] If while reading the brief the Court detects the distinct scent of candy canes and tears, it is because the brief was completed on the last business day before Christmas. The accused infringers refused to allow a one business day extension of the filing date. While not an issue for the lawyers, it seemed quite unfair – even Grinch-like – to the legal staff for TPL's counsel, who were compelled to work late into the evening to complete the filing.

[2] http://spectrum.ieee.org/semiconductors/processors/25-microchips-that-shook-the-world/5

TPL and Patriot have ownership interests in the Asserted Patents, hence their role in this case. TPL also develops microprocessors using the claimed technology, while Patriot markets and enables innovative proprietary technologies.

B. The Patented Technology.

The Asserted Patents share the same specification (with slight pagination differences). In their initial application, Moore and Fish provided elegant solutions to problems that had bedeviled the microprocessor industry for years. Their fundamental solutions are widely used today.

The four Asserted Patents have been the subject of at least 16 *ex parte* reexamination challenges before the U.S. Patent and Trademark Office ("PTO"), including three filed by Plaintiff HTC. The first '336 patent reexamination certificate issued on December 15, 2009; the second reexamination certificate issued on November 3, 2010. Collectively, the '336 patent was allowed over 607 prior art references that were cited in reexamination, including Judge Ward's claim construction order from the earlier Texas litigation, and the associated briefing and evidence. *See* Mar Decl., Exh. H (Reexam. Cert. for '336 patent). Similarly, the PTO recently issued reexamination certificates for: (i) the '890 patent over 614 cited references (Otteson Decl., Exh. AA); (ii) the '749 patent over 846 cited references (Otteson Decl., Exh. BB); and (iii) the '148 patent over 382 cited references (Otteson Decl., Exh. CC). To say that the claims of the Asserted Patents have been closely scrutinized by the PTO would be a vast understatement.

1. The '336 patent.

Microprocessors are complex machines with millions of individual parts whose operation requires coordination – both internally and with external components – for the chip to function properly. This coordination is enabled by clock signals. The '336 patent, entitled "High Performance Microprocessor Having Variable Speed System Clock," teaches the use of two independent clocks in a microprocessor system: (1) an on-chip first clock to time the CPU; and (2) a second independent clock to time the input/output (I/O) interface. This innovation was widely adopted by the industry and became fundamental to the increased speed and efficiency of modern microprocessors. Decoupling the system clock from the I/O clock allowed the clocks to run independently (or "asynchronously"), which permitted the CPU to run faster when needed.

2. The ’148 patent.

The ’148 patent, also entitled “High Performance Microprocessor Having Variable Speed System Clock,” teaches a microprocessor that combines an on-chip first clock with the use of more than 50% of the surface area of the integrated circuit for memory. This substantial increase in on-chip memory supports faster microprocessors, and potentially less expensive systems.

3. The ’890 patent.

The ’890 patent, entitled “High Performance, Low Cost Microprocessor Architecture,” teaches a dual stack architecture and the use of stack pointers that can reference memory in any location to provide more architectural flexibility and faster access to data elements. A stack architecture is sometimes analogized to a spring-loaded stack of plates of the kind used in a restaurant. The last plate placed (or “pushed”) on the top of the stack is the first plate removed (or “popped”) off the stack when needed. Like plates, data elements can be “pushed” onto or “popped” off the stack. However, by using a “stack pointer,” the CPU does not need to be an actual top-to-bottom “spring-loaded” stack. Instead, the stack pointer keeps track of where the “top of stack” item is in a “virtual stack,” so it can be accessed directly as if it were on the “top.”

Combining this with other features, such as a memory controller and direct memory access, the ’890 patent allows the CPU to off-load memory transfer of data to achieve further efficiencies and higher performance.

4. The ’749 patent.

Microprocessor instructions are usually stored in a memory that is slower than the CPU. The ’749 patent, entitled “High Performance, Low Cost Microprocessor Architecture,” teaches a processor that fetches multiple instructions at a time, and then supplies them to the CPU’s instruction register in parallel during the same memory cycle they are fetched. Since memory is generally slower than the CPU, being able to fetch and supply more than one instruction at a time increases the amount of instructions the CPU can receive in a given time, and thus increases instruction bandwidth.

C. The Prior Litigation and Claim Construction Ruling.

As the Court is aware, two of the Asserted Patents (the '336 and '148 patents) were the subject of prior litigation before Judge Ward in the Eastern District of Texas. Judge Ward construed some of the same claim terms at issue here (and other related terms), as discussed below. *See* Mar Decl., Exh. A (Judge Ward's *Markman* order) (Acer Dkt. 213-214).

Argument

I. THE LEGAL STANDARDS APPLICABLE TO CLAIM CONSTRUCTION.

A. General Principles of Claim Construction.

Claim interpretation is a legal issue that lies exclusively within the province of the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). To determine the meaning of claim terms, the Court must examine the intrinsic evidence: the claims, specification and file history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370, 116 S. Ct. 1384, 134 L. Ed. 2d 577 (1996); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The Court should begin the claim construction process by reviewing the claims. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*) ("It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'") (citation omitted). Claim terms are "generally given their ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." *Id.* at 1312-13 (citations omitted).

Claim terms are not be construed in a vacuum, however, "but in the context of the entire patent, including the specification." *Phillips* at 1313. Therefore, "claims 'must be read in view of the specification, of which they are a part.'" *Id.* at 1315 (citing *Markman*, 52 F.3d at 979). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id.* (citing *Vitronics*, 90 F.3d at 1582).

In addition to the claims and specification, it is necessary to review the prosecution history to determine whether the applicant has made "any express representations . . . regarding

the scope of the claims." *Vitronics*, 90 F.3d at 1582. Finally, if the proper interpretation of the claim is not clear from the intrinsic record, the court may rely on extrinsic evidence, which "is that evidence which is external to the patent and file history, such as expert testimony, inventor testimony, dictionaries, and technical treatises and articles." *Vitronics*, 90 F.3d at 1584. The Federal Circuit has emphasized: "Extrinsic evidence . . . such as expert testimony . . . may also be considered when appropriate as an inherent part of the process of claim construction and as an aid in arriving at the proper construction of the claim, but may not be used to vary or contradict the otherwise unambiguous meaning of the claim." *Desper Prods., Inc. v. QSound Labs, Inc.*, 157 F.3d 1325, 1333 (Fed Cir. 1998).

B. <u>The Doctrine of "Disavowal," which Plaintiffs Misapply</u>.

Plaintiffs rely on the doctrine "disavowal" for several of their proposed constructions. The "disavowal" doctrine is a rule of claim construction that is frequently invoked but rarely applicable. First, the doctrine only applies where the disavowal is "clear and unmistakable." *See Cordis Corp. v. Medtronic Ave, Inc.*, 511 F.3d 1157, 1177 (Fed Cir. 2008) ("alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable"). Second – and very important here – the alleged disavowal must be made by the ***patentee***, not the ***examiner***. *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1347 (Fed. Cir. 2005) ("[U]nilateral statements by an examiner do not give rise to a clear disavowal of claim scope by an applicant," as "the applicant has disavowed nothing."); *Univ. of Pittsburgh of Commonwealth System of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1296-97 (Fed. Cir. 2009) ("A wide chasm exists between the weak inference from the [interview] summary . . . and a clear and unmistakable disavowal as required to limit a claim term.")

C. <u>It Is Improper to Import Limitations from the Specification Into the Claims</u>.

While claim limitations must be construed in light of the specification and prosecution history, it is improper to import limitations into the claims where such limitations are not present in the language of the claim itself. *Phillips*, 415 F.3d at 1323. A difference exists between construing a term appearing in a claim versus adding a limitation that does not appear in the claim in the first instance. The former is permissible, while the latter is not. *See, e.g.*,

Interactive Gift Express, Inc. v. Compuserve, Inc., 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("in looking to the specification to construe claim terms, care must be taken to avoid reading 'limitations appearing in the specification . . . into [the] claims'") (citations omitted); *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999) ("Consistent with the principle that the patented invention is defined by the claims, we have often held that limitations cannot be read into the claims from the specification or the prosecution history").

Although the specification may indicate that certain embodiments are preferred, references to preferred embodiments are not claim limitations. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002) ("the number of embodiments disclosed in the specification is not determinative of the meaning of disputed claim terms").

II. TPL'S CONSTRUCTION OF THE "TOP TEN" DISPUTED TERMS IS CONSISTENT WITH THE INTRINSIC EVIDENCE AND THE UNDERSTANDING OF ONE OF ORDINARY SKILL IN THE ART.

The parties dispute the proper construction of multiple claim terms from the Asserted Patents. In nearly every instance, the dispute centers on Plaintiffs' attempts to import limitations into a claim that would either limit the claim to a preferred embodiment or exclude a preferred embodiment. The Court has ordered that only 10 terms be construed; those 10 disputed terms, their proposed constructions, and their support, are specified in the parties' JCCS and related Exhibits B-D (Acer Dkt. 307, 305). Those terms were also previously discussed in Defendants' Opening Claim Construction Brief and subsequent response brief (Acer Dkt. 221, 227).

A. <u>The Proper Construction of "Multiple Sequential Instructions" ('749 Patent)</u>.

The parties dispute the meaning of "multiple sequential instructions," found in claims 1, 9, 43, 44, 45, 47, and 59 of the '749 patent. The parties' competing constructions are as follows; differences are noted in bold and strike-through:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
multiple sequential instructions	Two or more instructions in ~~program~~ sequence**, in which any operand that is present must be right-justified in the instruction register**	Two or more instructions in a program sequence

One aspect of the invention concerns avoiding the so-called "Von Neumann bottleneck," which relates to a practical barrier in the speed of providing program instructions from memory to the CPU. One approach to surmounting the bottleneck is to fetch multiple instructions from memory during a single memory cycle, as opposed to a single instruction during each memory cycle. In one embodiment, the '749 patent teaches the fetching of four instructions per memory cycle, where each instruction is in 8-bit format. Thus, a microprocessor with a 32-bit instruction register that processes 8-bit instructions four at a time could run four times faster. *See, e.g.*, '749 patent, 5:54-58, 7:12-18. When viewed in this context, the phrase "multiple sequential instructions" is straightforward, requiring little to no construction beyond its ordinary meaning, as TPL proposes. Rather than accept the plain and ordinary meaning of the phrase, Plaintiffs seek to add the extraneous limitation "in which any operand that is present must be right-justified in the instruction register." JCCS Row 7.

TPL's construction follows the guidance of *Phillips*, 415 F.3d at 1312, where the words used in a claim are generally given their ordinary and customary meaning. Here, "multiple" means "two or more," and "sequential instructions" means "instructions in a program sequence." Plaintiffs' proposal goes beyond the claimed sequential instructions in an attempt to sweep in instruction registers themselves, and operands within those registers. This approach conflicts with the controlling guidance of *Phillips* and should be rejected.

Plaintiffs' misplaced justification for narrowing the claim phrase follows from Judge Ward's previous construction of a different patent (the '584 patent); specifically, the term "instruction groups" and how those groups are arranged in an "instruction register." [3] The '584 patent is a divisional patent of the '749 patent, meaning the '584 patent carves out separate subject matter from its parent, the '749 patent. The "instruction groups" claim term in the '584

[3] Plaintiffs' look to Judge Ward's claim construction of "instruction groups" from the '584 patent to construe "instruction register" in the '749 patent, ignoring that the parties in that case stipulated to a separate construction of "instruction register" that did not require operands to be right-justified: "[i]nstruction register means a hardware element that receives and holds an instruction group as it is extracted from memory; the register either contains or is connected to circuits that interpret the instructions in the group." Ward 8, Mar Decl., Exh. A.

patent refer to how instructions and data are organized in memory; the '749 patent claims how multiple sequential instructions are supplied to the CPU in a single memory cycle. Plaintiffs ignore the significant distinctions between the claims of the two patents, as they must, because it is the *claims* of a patent that define the scope of the invention.

Unlike the '584 patent, the '749 patent claims "multiple sequential instructions". The claimed multiple sequential instructions are not the same as the '584 patent's "instruction groups" for at least the simple reason there is no limitation in the '749 claims requiring an operand as is the case in, for example, claim 29 of the '584 patent. Moreover, there is no limitation in the claims of the '749 patent that even implicitly require such hypothetically present operands be right justified because, in contrast to claim 29 of the '584 patent, there is no that requirement any operand be located at a "predetermined position." Thus, Judge Ward's construction of "instruction groups," with its limitation on operands in the context of a claim directed to "certain instructions," is inapplicable here.

For the foregoing reasons, TPL's proposed construction should be adopted.

B. <u>The Proper Construction of "Separate Direct Memory Access Central Processing Unit" ('890 Patent)</u>.

The parties dispute the proper construction of the term "separate direct memory access central processing unit," as follows:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
separate direct memory access central processing unit	a separate CPU that fetches and executes instructions for performing direct memory access without using the main CPU	electrical circuit for reading and writing to memory that is separate from a main CPU

A straightforward reading of claim 1 of the '890 patent provides for: (i) a main central processing unit (or main CPU); and (ii) a direct memory access central processing unit (or DMA CPU) that is separate from the main CPU:

> A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said

> microprocessor, . . . said direct memory access central processing unit providing inputs to said memory controller . . .

'890 patent, 32:44-47 (Mar Decl., Exh. K). The plain meaning of the claim language is confirmed by the '890 specification, which describes and illustrates a main CPU and a separate DMA CPU in a single integrated circuit making up a microprocessor. '890 patent, 6:17-20. The parties agree that "CPU" means "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." (JCCS Ex. A, No. 7 Dkt. 305).

Given the foregoing, construction of the term should be straightforward based on ordinary meaning of the claimed structure, and TPL's proposed construction captures the essence of such ordinary meaning. Plaintiffs, on the other hand, do not offer a structural definition of the claimed term. Instead, they restate the term with extraneous functional limitations that are not supported by the specification, in particular, prohibiting ***any*** operation of the DMA with assistance, no matter how minor, of the main CPU. Yet the claim language includes no such prohibition, nor is there support for such limitation in the specification. In contrast, TPL's construction is correct because it describes the "DMA CPU" as properly distinct ("separate") from the main CPU, in keeping with the claim structure, and defines the DMA CPU in accordance with the specification, as an "electrical circuit for reading and writing to memory."

The specification includes at least two preferred embodiments of the DMA CPU. The first is shown in Figure 2, where the microprocessor 50 has a separate DMA CPU 72 with "the ability to fetch and execute instructions." '749 patent, 8:22-23; Mar Decl., Exh. M. "[A] second embodiment of a microprocessor in accordance with the invention," shown in Figure 9, discloses a DRAM die with on-chip memory and a "DMA CPU" 314. *Id*., 4:61-62. Here, "the DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller." *Id*., 12:63-65 (emphasis added). This "more traditional DMA controller" is one that functions more as a traditional state machine, without the ability to fetch its own instructions that characterizes a CPU. *See, e.g., id*., 1:55-58, Background of the Invention (DMA controllers in conventional microprocessors "can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.").

The specification discloses at least two embodiments of a DMA CPU, while Plaintiffs' construction would exclude the "traditional" "DMA CPU 314" of Figure 9.

Plaintiffs attempt to narrow the ordinary meaning of DMA by limiting it to "performing direct memory access without using the main CPU" is incorrect, as such would exclude a preferred embodiment. Indeed, even Plaintiffs' expert, Dr. Wolfe, testified that the main CPU can initiate memory transfers.[4] As this falls within the realm of "direct memory access related operations," even Plaintiffs' expert appears to disagree with Plaintiffs' proposal. TPL's construction properly captures the breadth of this term.

C. <u>The Proper Construction of "Instruction Register" ('890 and '749 Patents)</u>.

The parties dispute the proper construction of the term "instruction register" found in the '749 and '890 patents. Here, just as with "multiple sequential instructions," Plaintiffs improperly insert the extraneous phrase "in which any operand that is present must be right-justified in the register."

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
instruction register	register that receives and holds one or more instructions for supplying to circuits that interpret the instructions**, in which any operand that is present must be right-justified in the register**	register that receives and holds one or more instructions for supplying to circuits that interpret the instructions

This term is found in claim 1 of the '890 patent and claim 1, 47, and 59 of the '749 patent. As with the term "multiple sequential instructions," the term "instruction register" has a common meaning that can be understood from the phrase itself. As described by the '749 patent, an instruction register merely receives instructions – *e.g.*, in a preferred embodiment, the register receives four 8-bit instruction words on a 32-bit internal data bus. '749 patent, col. 7:36-41.

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[4] "Q. [Can the main CPU in the '890 patent] [i]nitiate a transfer or request for data from memory?"
"A. Well, it certainly can request a single element of data from memory, that's one of its capabilities, yeah." Wolfe Depo. 167:19-168:10 (Mar Decl., Exh. V).

The parties agree on the first portion of the construction: "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions". This is not surprising in that the definition comports precisely with the specification and the ordinary meaning of the term. But as explained with reference to the term "multiple sequential instructions," Plaintiffs improperly seek to narrow this plain and ordinary construction through importation of the same wholly extraneous limitation from Judge Ward's construction of the '584 patent discussed above – "**in which any operand that is present must be right-justified in the register."** For the reasons previously discussed, the Court should adopt TPL's proposed construction.

D. <u>The Proper Construction of "Operates Asynchronously To" ('336 Patent)</u>.

The term "operates asynchronously to" is found in claims 11, 13 and 16 of the '336 patent. The specification section entitled "ASYNCHRONOUS / SYNCHRONOUS CPU" explains that "[m]ost microprocessors derive all system timing from a single clock." '336 17:12-13. The section goes on to describe "a dual clock scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface." The asynchronous operation of the CPU and I/O interface is due to the fact that the two devices are timed by two independent clock signals, as shown in FIG.17 (at right).

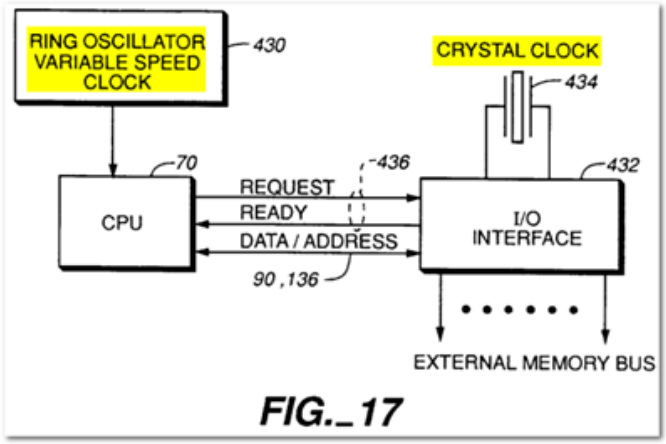


FIG._17

For example, Claim 11 of the '336 patent recites:

> an entire ring oscillator variable speed system clock … connected to said [CPU] …. and a second clock ***independent*** of said ring oscillator variable speed system clock connected to said input/output interface, ***wherein*** said central processing unit ***operates asynchronously to*** said input/output interface.

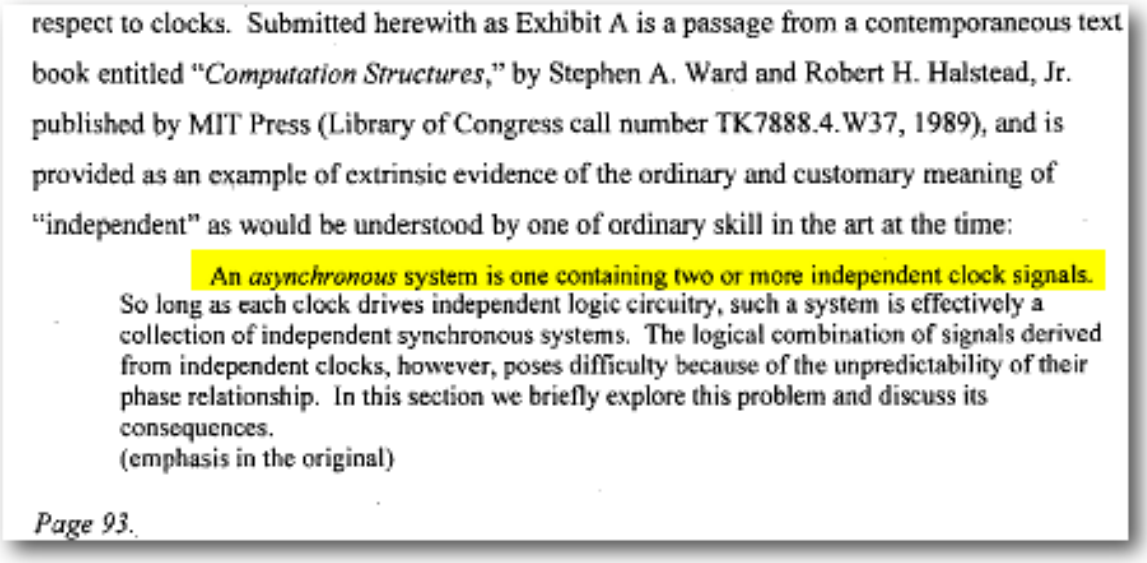
The "wherein" clause of Claim 11 describes the result of timing the CPU and I/O by independent clocks. By employing independent clocks, the CPU is not limited or capped by the I/O clock, enabling faster performance. '336 patent 17:32-34 ("By decoupling the variable speed

of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each.") This does not mean there is *no* timing relationship.

The parties' competing constructions are as follows:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
operates asynchronously to	operates without a timing relationship to/with	timed by independent clock signals

The applicants introduced "asynchronously" during prosecution "to clarify the meaning of 'independent' as recited in the claims." '336 Reexam Hist. (Mar Decl., Exh. G at TPL0549470-71). The Examiner had focused on the Kato reference that purported to show two clocks. Mar Decl., Exh. F at TPL0553772. The applicant explained that the claims referred to two "independent" clocks, and not a second clock derived from a first as in Kato. *Id.* In support of this explanation, the applicant cited a textbook that defined "an asynchronous system" as "one containing two or more independent clock signals." *Id.* at TPL0553776:



respect to clocks. Submitted herewith as Exhibit A is a passage from a contemporaneous text book entitled "*Computation Structures*," by Stephen A. Ward and Robert H. Halstead, Jr. published by MIT Press (Library of Congress call number TK7888.4.W37, 1989), and is provided as an example of extrinsic evidence of the ordinary and customary meaning of "independent" as would be understood by one of ordinary skill in the art at the time:

> An *asynchronous* system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems. The logical combination of signals derived from independent clocks, however, poses difficulty because of the unpredictability of their phase relationship. In this section we briefly explore this problem and discuss its consequences.
> (emphasis in the original)

Page 93.

Thus, the applicant acted as his own lexicographer – albeit by providing the PTO with a standard definition – and recited essentially the same construction that Defendants propose now.[5]

[5] Plaintiffs' expert Dr. Wolfe agrees that asynchronous and independent "mean[] pretty much the same thing." Wolfe Depo., 134:8-11 (Mar Decl. Exh. V).

In view of this evidence, "timed by independent clock signals" properly captures the meaning of "operates asynchronously to" in the claims of the '336 patent.[6]

There is no specification support for Plaintiffs' proposed requirement that the CPU "operates without a timing relationship to/with" the input/output interface, and indeed Plaintiffs cite none. That is because all clocks have ***some*** timing relationship to one another due to their periodic nature. For example, in a two-clock system, one clock will run X times faster than the other clock, thereby having a "timing relationship," whether intentional or not. Thus, Plaintiffs' proposed construction would exclude not just the preferred embodiment but ***all*** embodiments, and must be rejected.

E. <u>The Proper Construction of "Supply the Multiple Sequential Instructions to Said Central Processing Unit Integrated Circuit During a Single Memory Cycle" ('749 Patent)</u>.

This term is found in claim 1 of the '749 patent. Plaintiffs' proposed construction differs from TPL's in that Plaintiffs improperly seek to add extraneous limitations.

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle	provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide buffer that supplies one instruction at a time**	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The phrase under construction is again straightforward based on its plain language: "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." To put the phrase in context, once the multiple sequential instructions have been fetched, the instructions are supplied to the central processing unit, where both the fetch and supply occur during a single memory cycle. The fact that the parties agree on

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[6] *See also*, '336 Reexam. Hist. (Mar Decl., Exh. F at TPL0553771-785; Exh. G at TPL0549461-462, TPL0549464, TPL0549467-473; Exh. H at TPL0548763 ('336 Reexam. Cert., col. 1 (replacing col. 17, ll. 12-37)).

the use of the words "in parallel" follows from a companion limitation that provides the multiple sequential instructions are fetched in parallel.

Once again, however, Plaintiffs improperly seek to narrow the claim by importing extraneous limitations into the plain language, particularly with respect to the phrase "**without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies one instruction at a time**." Neither the claim nor the specifications supports Plaintiffs' attempt to exclude prefetch or one-instruction-wide buffers. Importantly, the specification does not exclude systems with prefetch buffers or one-instruction-wide buffers, and none of Plaintiffs' intrinsic evidence cited in the JCCS suggests that it does. Rather, the patent merely teaches preferred embodiments with the ability to fetch and supply multiple instructions in parallel in a single cycle without using an intervening prefetch buffer.

This observation is further supported by the prosecution history. During reexamination, the inventors overcame a rejection for anticipation based on the Transputer references: Edwards and May. While the Transputer references disclosed fetching instructions into a prefetch buffer, the instructions were not supplied to the instruction register until a second memory cycle, thus distinguishing the references from the '749 patent. The inventors traversed the rejection by noting that "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'" '749 Reexam. Hist. (Mar Decl., Exh. Q at TPL0554266). The traverse does not mean that using a prefetch buffer to fetch multiple instructions is not within the claim scope; the key is having the capability to fetch and supply multiple sequential instructions in a single memory cycle. While the Transputer references disclose a memory controller that fetches multiple instructions, it supplies them only one at a time, and therefore does not meet the claim limitation.[7]

[7] May discloses parallel register banks, but because it has only one instruction buffer that holds only one instruction, all instructions must pass through that single buffer, and only one instruction at a time is supplied to the CPU. '749 Reexam. Hist. (Mar Decl., Exh. R at TPL-VO007138).

The language of amended claim 1, which emerged from reexamination on June 7, 2011 confirms this point. The amended claim makes clear that the claimed means to fetch multiple sequential instructions from memory in parallel and supply them during a single memory cycle merely involves "supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched." '749 Reexam Hist. 1/25/11 Amendment (Mar Decl., Exh. B), at 2. The PTO did not require limiting language about prefetch or one-instruction-wide buffers. Plaintiffs' attempt to improperly narrow the claim should be rejected.

F. The Proper Construction of "Clocking Said Central Processing Unit" ('336 Patent).

The parties dispute the proper construction of the term "clocking said central processing unit." The term appears in the '336 patent claims to explain that the on-chip clock provides the timing for the CPU.

Plaintiffs seek to add limitations indicated in bold below:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
clocking said central processing unit	timing the operation of the CPU **such that it will always execute at the maximum frequency possible, but never too fast**	timing the operation of the CPU

The complete claim phrase that this term appears in is:

"an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator **clocking said central processing unit.**"

Judge Ward construed a different portion of this phrase, but that construction is highly relevant. Judge Ward construed the portion that reads "said oscillator clocking" or "oscillator … clocking" as **"an oscillator that generates the signal(s) used for timing the operation of the CPU."** Ward Order at 13 (Mar Decl., Exh. A). The parties here have agreed to that construction. *See* Acer Dkt. 305, Exh. A, Agreed Construction No. 19 (excerpted on the following page):

19.	oscillator . . . clocking [Claims 1, 6, 10]	an oscillator that generates the signal(s) used for timing the operation of the CPU	an oscillator that generates the signal(s) used for timing the operation of the CPU

TPL's proposed construction matches the latter half of Judge Ward's construction, because TPL is only construing the latter half of the phrase so that it is consistent with Agreed Construction No. 19. Plaintiffs' own expert agrees. Wolfe Dep. 135:20-24 (Mar Decl. Exh. V) ("general ordinary meaning would have been providing an oscillating signal that can be used as a timing reference for the circuits in the central processing unit, basically providing a clock").

Plaintiffs want to add an additional limitation: "such that it will execute at the maximum frequency possible but never too fast." This is language taken from the '336 at 16:59-17:2, wherein the patentee is generally describing an advantage of the preferred embodiment. However, it is improper to import limitations from the specification into the claims. *Phillips*, 415 F.3d at 1323.

G. <u>The Proper Construction of "Ring Oscillator" ('148, '336, '890, '749 Patents)</u>.

The patents teach that a ring oscillator is a way to implement an on-chip clock. *See e.g.*, FIG. 17 (excerpt below).

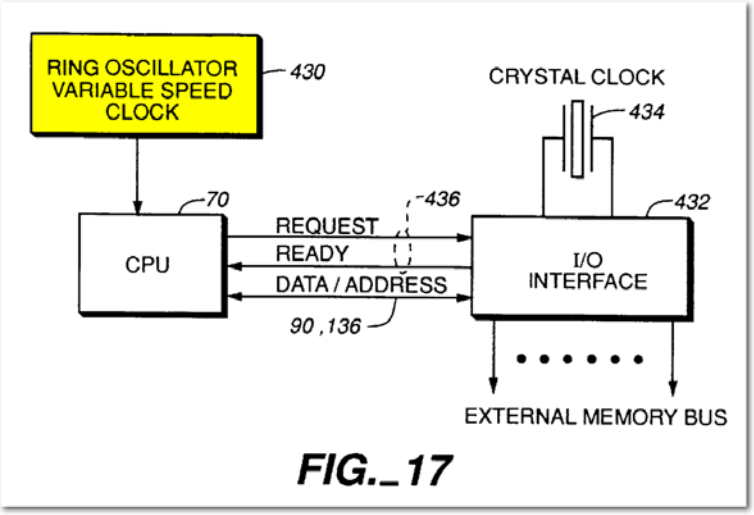

FIG._17

The term "ring oscillator" is found in claims 1, 9, 11, and 15 of the '336 patent, in claim 7 of the '890 patent, and in claims 4 and 11 of the '148 patent. Judge Ward construed ring oscillator

in the manner TPL proposes: "An oscillator having a multiple, odd number of inversions arranged in a loop." Ward Order at 11 (Mar Decl., Exh. A). Plaintiffs agree with that portion of the construction, but seek to add two additional limitations, as shown in bold below:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
ring oscillator	an oscillator having a multiple, odd number of inversions arranged in a loop, **wherein the oscillator is: (1) noncontrollable; and (2) variable based on the temperature, voltage, and process parameters in the environment**	an oscillator having a multiple, odd number of inversions arranged in a loop

The additional limitations proposed by Plaintiffs are taken from the examiner's summary of an interview during the reexamination of the '148 patent. In the interview summary describing the "general nature" of what was discussed, the examiner stated that the applicant discussed these features of a ring oscillator, and argued that they overcame a reference by Talbot. Otteson Decl., Exh. X. The complete examiner summary – which the Plaintiffs incorrectly argue to be a "disavowal" – is shown below.

Continuation of Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Discussed differences in the prior art and the claimed invention. Particularly, the patent owner argued that the references failed to teach of the limitation requiring "said memory further occupying a majority of the total area of said single substrate". The patent owner further pointed out that the reference of May, noted above, describes that the memory can be the largest and densest component on the chip, but this is different than being the "majority of the total area",

Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator". The patent owner discussed features of a ring oscillator, such as being non-controllable, and being variable based on the environment. The patent owner argued that these features distinguish over what Talbot teaches. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992

Whatever the examiner might have meant by this language, it is far more important to understand what occurred next. As the examiner noted, the February 12, 2008 interview

included a discussion of the Talbot reference. The examiner and the patent owner agreed that "[t]he examiner will reconsider the current rejection [premised on Talbot] based on a forthcoming response, which will include arguments similar to what was discussed." Within eight days of the interview (dated February 21, 2008, but filed February 26, 2008) TPL submitted the promised written response. Otteson Decl., Ex. Y. This written response explained in detail why Talbot was distinguishable, and importantly *did not* make the arguments that Plaintiffs seek to insert into the claim construction here.

Even more importantly, in an action dated June 25, 2008, the examiner expressly accepted the arguments contained in the written response, never mentioning the interview. Specifically, the examiner stated "Patent Owner's arguments, filed 2/26/08 with respect to the rejections [based on Talbot] have been fully considered and are persuasive. Therefore, the rejection … has been withdrawn." Otteson Decl., Ex. Z. Thus, the examiner expressly relied on the patent owner's written arguments to overcome Talbot, and ***not*** the interview.

Moreover, Plaintiffs' proposed limitation of "variable based on the temperature, voltage, and process parameters in the environment" and "non-controllable" are contradictory, because temperature, voltage and process are all controllable to one degree or another, and therefore the oscillator is controllable via these parameters. According to the '336 specification, "the ring oscillator frequency is determined by the parameters of temperature, voltage, and process." *Id*., 16:59-60. It makes no sense that the oscillator frequency can be "determined by" temperature, voltage and process," while simultaneously being uncontrollable. Indeed, claim 13 of the '336 patent calls for "clocking said central processing unit at a clock rate," which would be impossible if the oscillator were uncontrollable. For all of these reasons, Plaintiffs proposal should be rejected.

H. <u>The Proper Construction of "Providing an Entire Variable Speed Clock Disposed Upon Said Integrated Circuit Substrate" ('336 Patent)</u>.

The issue here is the degree of independence between the external reference signal and the on-chip clock. Judge Ward construed this term in a manner that excludes systems where the on-chip clock directly relies on a command input control signal or external crystal/clock to generate a

clock signal. Plaintiffs seek to further construe Judge Ward's construction to add the additional limitations indicated in bold and strike-out:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
providing an entire variable speed clock disposed upon said integrated circuit substrate	providing a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and **does not ~~directly~~ rely** on a ~~command input~~ control signal or an external crystal/clock generator to generate a clock signal, **wherein the variable speed clock is: (1) noncontrollable; and (2) variable based on the temperature, voltage, and process parameters in the environment**	providing a variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and **does not directly rely** on a **command input** control signal or an external crystal/clock generator to generate a clock signal

First, Plaintiffs seek to apply their "examiner disclaimer" theory from "ring oscillator" (Section II. G, above) to the term "variable speed" clock, even though the terms are different and "variable speed clock" was not at issue in the '148 patent reexamination. The reasons Plaintiffs' "examiner disclaimer" theory fails with respect to "ring oscillator" apply with even greater force here. One cannot infer a "clear and unmistakable disavowal" from an examiner's comment concerning a different term in a different patent.

Next, Plaintiffs seek to narrow Judge Ward's construction by broadening the exclusions. The Texas defendants argued that the patentee disclaimed ***any*** use by the on-chip oscillator of an external reference signal. Ward Order at 11 (Mar Decl. Exh. A). Judge Ward rejected that argument, and declined to exclude any use of an external clock as a reference signal. Instead, Judge Ward determined that any disclaimer was limited to an on-chip ring oscillator that "***directly*** relied on a ***command input*** control signal or an external crystal/clock generator ***to generate a clock signal***." *Id*. at 12 (emphasis added). Judge Ward thus construed the term to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU **and does not *directly* rely on a *command input* control**

signal or an external crystal/clock generator *to generate a clock signal* - the same construction Defendants now propose. Ward Order, p. 12 (Mar Decl. Exh. A) (emphasis added).

Plaintiffs' attempt to broaden the disclaimer by modifying Judge Ward's construction should be rejected.

I. The Proper Construction of "Push Down Stack Connected to Said ALU" ('749 Patent).

The parties dispute the proper construction of the term "push down stack connected to said arithmetic logic unit [("ALU")]."

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
push down stack connected to said ALU	a push down stack comprising a top item register and a next item register, both directly coupled to the ALU such that the source and destination addresses are not used	data storage elements organized to provide last-in first-out access to items connected to convey signals to a digital circuit that performs both arithmetic and logical operations.

Construction of this phrase requires focus on the meaning of "push down stack" and the manner in which the stack is "connected to" the claimed ALU. The parties agree on the meaning of "ALU" – "a digital circuit that performs arithmetic and logical operations." The parties also partially agree that a "push down stack" – also referred to as a "stack" – consists of data storage elements organized to provide last-in, first-out ("LIFO") access to items. *See, e.g.*, '890 Reexam Hist. (Mar Decl., Exh. L at TPL-VO004406) ("stack is sometimes referred to as a last-in-first-out or LIFO data structure"); *see also*, The Computer Glossary, 651 (Mar Decl., Exh. S). This last-in-first-out property is also expressed in terms of "pushing" and "popping." "The last item, or address, placed (pushed) onto the stack is the first item removed (popped) from the stack." *Id.* The disagreement arises through Plaintiffs' improper attempt to add the extraneous limitations "directly coupled" (rather than simply "connected to") and "such that source and destination addresses are not used." These extraneous limitations are not required or supported by the claim language or the specification, and should, thus, be rejected.

The patents disclose a variety of stacks that provide data to an ALU. *See, e.g.*, Figures 2, 13 and 21. Figures 2 and 13 both illustrate connections to an ALU. Figure 2 illustrates dedicated registers that provide inputs to the ALU. Figure 13, on the other hand, does not illustrate dedicated registers. Rather, the stack elements themselves are connected to the ALU as indicated by the stack pointer. Plaintiffs' construction improperly seeks to limit the construction of "push down stack" to the embodiment illustrated in Figure 2. The claim language does not, however, so limit the connection of the stack to the ALU through dedicated registers. In other words, a "direct coupling" is not required.

Furthermore, none of the embodiments discuss how pieces of data are physically arranged or physically propagate from element-to-element either within the stack or to the ALU upon a push or a pop. To the contrary, some use embodiments general purpose memory such as RAM to store data items. *See, e.g.*, Figure 21. Most, if not all, embodiments use stack pointers to track the contents of and operate the stacks. As discussed, Figure 2 discloses a push down stack (74) connected to separate top and next item registers (76 and 78). However, Figure 13 shows a stack that does not have separate physical top and next registers. Rather it has a stack pointer that designates which of many randomly accessed elements is top or next. Which of the randomly accessed elements is top, or which is next, is determined by the stack pointer. Further, having stack pointers "point to" a randomly accessed data storage element would be unnecessary if the data were always physically stacked in a single location and propagated from element-to-element as Plaintiffs propose in their definition of "push down stack."

Figure 21 drives this point home, showing a novel triple cache stack architecture utilizing on-chip and off-chip memory including RAM to store stack elements, which are addressed by stack pointers. *Id.*, 19:6-43. RAM is, by definition, "random access memory." Such memory does not "propagate" stack items in any physical way through RAM. The elements of this stack are organized by the microprocessor using multiple stack pointers.[8] *Id.*, 19:20-23; 35-38.

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[8] *See* The Computer Dictionary (stack pointer: "A register that contains the current address of the top element of the stack"). Mar Decl., Exh. T.

The output destination of the Figure 21 embodiment is not stated. Implicitly, it could be either that of Figure 2 or that of Figure 13, one utilizing dedicated registers or one that does not. In the case of Figure 13, Figure 21 suggests any random access element may be connected to the ALU, including the on chip latches illustrated in Figure 21 that receive data from off chip memory, as illustrated.

In sum, the preferred embodiments include instances of direct and indirect coupling between the push down stack and ALU. Further, these embodiments include the use of source and destination registers in providing data from the stack to the ALU. Plaintiffs' claim construction would read out these embodiments, particularly those illustrated by Figures 13 and 21. Plaintiffs' construction is, therefore, improper. *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1377 (Fed. Cir. 2005) (reading out preferred embodiment "would rarely if ever be correct.").

J. <u>The Proper Construction of "As a Function of Parameter Variation" ('336 Patent)</u>.

The parties dispute the proper construction of the term "as a function of parameter variation." The specification for the '336 patent describes a problem with traditional CPU designs as follows:

> Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse (sic) case of the three parameters, the circuit will function at the rated clock speed. The results are (sic) designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions. ['336 patent at 16:47-54]

The '336 patent addresses this concern by placing the ring oscillator on the same silicon substrate as the CPU. '336 patent, 16:57-58. ("The clock is fabricated on the same silicon chip as the rest of the microprocessor 50.") That way, the ring oscillator and CPU will be similarly affected. *Id.* at 16:63-68 ("The ring oscillator 430 is useful as a system clock … because its performance tracks the parameters which similarly affect all other transistors on the same silicon die.")

Defendants propose that the processing frequency and clock rate vary "based on a parameter variation." Plaintiffs seek to propose an additional deterministic relationship. The disagreement is shown below:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
as a function of parameter variation	in a determined functional relationship with parameter variation	based on parameter variation

As always, it is important to understand the context in which this term arises. The complete limitation of claim 6 of the '336 patent that contains this term recites:

> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way ***as a function of parameter variation*** in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

'336 Reexam Cert., 2:22-28 (Mar Decl., Exh. H) (emphasis added). The first thing to note is that the term in question is preceded by the word "thus …" so the term is describing the ***result*** of placing the entire oscillator on the same integrated circuit substrate. Read in context, the term simply means that as fabrication OR operational parameters vary – such as either voltage, temperature or process technology – the CPU frequency and oscillator clock will also vary. There is no requirement of a deterministic relationship.

Plaintiffs' proposed construction would require a "determined functional relationship." This construction suggests the existence of an algebraic function to predict the CPU frequency and clock rate, even though **no** such mathematical relationship is disclosed in the specification. Plaintiffs' construction is also confusing because: (a) it construes "function" by relying on the word "functional," which is circular and unhelpful; and (b) it uses the phrase "functional relationship," which the PTO used in a completely different sense during prosecution. *See e.g.*, '336 Pros. Hist. (Mar Decl., Exh. C at TPL0001903) (specifying "functional relationship" as "ring oscillator variable speed system clock is disposed to clock the central processing unit"). Plaintiffs' construction should be rejected.

Plaintiffs take an overly restrictive position by requiring that the parameter variation be "determined." Plaintiffs concede, however, that the specification describes no algebraic functions

relating temperature, voltage, and process. In fact, there is a degree of randomness with microprocessors (even the support used by Plaintiffs states "the frequency will be in the neighborhood of …"). Indeed, over time permutations in the microscopic structure of the integrated circuit can cause performance changes. Furthermore, Plaintiffs do not dispute that their construction is confusing and contradicts the sense in which "functional relationship" was used in prosecution. For all of these reasons, TPL's proposal should be adopted.

Conclusion

For the foregoing reasons, Defendants respectfully ask the Court to enter an order adopting TPL's proposed claims constructions.

Dated: December 23, 2011

Respectfully submitted,

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